IN THE CLAIMS

Please amend claims 1, 5, and 9 as follows:

1(Amended). A method for forming interconnects, comprising:

providing a silicon substrate containing one or more electronic devices;

A1 forming a first dielectric layer over said silicon substrate;

forming a second dielectric layer over said first dielectric layer wherein the dielectric constant of the second dielectric layer is less than 3.0;

forming a first hardmask layer over said second dielectric layer;

forming a second hardmask layer on said first hardmask layer wherein said second hardmask layer comprises a material selected from the group consisting of titanium aluminide (TiAl), titanium aluminum nitride (TiAlN), titanium nitride (TiN), aluminum nitride (AlN), tantalum aluminide (TaAl), and tantalum aluminum nitride (TaAlN);

forming a trench in said second dielectric; and

filling said trench with a conducting material.

5 (Amended). A method for forming interconnects, comprising:

A2 providing a silicon substrate containing one or more electronic devices;

forming a first dielectric layer over said silicon substrate;

forming a second dielectric layer over said first dielectric layer wherein the dielectric constant of the second dielectric layer is less than 3.0;

forming a first hardmask layer over said second dielectric layer;

A2 cont.

forming a second hardmask layer on said first hardmask layer wherein said second hardmask layer comprises a material selected from the group consisting of titanium aluminide (TiAl), titanium aluminum nitride (TiAlN), titanium nitride (TiN), aluminum nitride (AlN), tantalum aluminide (TaAl), and tantalum aluminum nitride (TaAlN);

etching a first opening in said second hardmask layer of a first width;

forming a first trench of a second width in said second dielectric layer wherein said second width is less than said first width;

etching a second opening in said first hardmask layer of a first width;

forming a second trench of a first width in said second dielectric layer wherein said second trench is positioned over said first trench; and

filling said first and second trenches with a conducting material.

---

9 (Amended). A method for forming interconnects, comprising:

A3

providing a silicon substrate containing one or more electronic devices;

forming a first etch stop layer over said silicon substrate;

forming a first dielectric layer over said first etch stop layer wherein the dielectric constant of the first dielectric layer is less than 3.0;

forming a second etch stop layer over said first dielectric layer;

forming a second dielectric layer over said second etch stop layer wherein the dielectric constant of the second dielectric layer is less than 3.0;

A3 cont.

forming a first hardmask layer over said second dielectric layer;

forming a second hardmask layer on said first hardmask layer wherein said second hardmask layer comprises a material selected from the group consisting of titanium aluminide (TiAl), titanium aluminum nitride (TiAlN), titanium nitride (TiN), aluminum nitride (AlN), tantalum aluminide (TaAl), and tantalum aluminum nitride (TaAlN);

etching a first opening in said second hardmask layer of a first width;

forming a first trench of a second width in said second dielectric layer wherein said second width is less than said first width;

etching a second opening in said first hardmask layer of a first width;

forming a second trench of a first width in said second dielectric layer wherein said second trench is positioned over said first trench;

simultaneously etching said second trench to a depth of said second etch stop layer and said first trench to a depth of said first etch stop layer; and

filling said first and second trenches with a conducting material.